AMENDMENTS TO THE CLAIMS

Please amend the claims as indicated below.

Please cancel claim 1 without prejudice.

This listing of claims will replace all prior versions, and listings, of claims in the application:

Listing of Claims:

Claim 1 (withdrawn): A field effect transistor in which at least one vertically aligned semiconductor column (2) of a diameter in the nanometer range is present between a source electrode and a drain electrode (1, 7) and is annularly surrounded by a gate electrode with an insulating space between them,
characterized by the fact that
the semiconductor columns (2) are embedded in a first and a second insulating layer (3,5) between which there is provided a metal layer (4) extending to the outside as a gate electrode whose ends penetrating through the second insulating layer (5) are partially converted to an insulator (6) or partially removed and filled by an insulating material.

Claim 2 (currently amended): A method of fabricating a field effect transistor in which at least one vertically aligned semiconductor column ~~(2)~~ of a diameter in the nanometer range is present between a source electrode and a drain electrode ~~(1, 7)~~ and is annularly surrounded by a gate electrode with an insulating space between them,
~~characterized by the fact that~~ the method comprising:

- free-standing semiconductor columns are grown vertically on a conductive substrate;
- a first insulating layer is deposited on the semiconductor columns;
- a first conductive metal layer and a second insulating layer are deposited thereon;
- the developing laminate ~~laminates~~ is etched planar to the point of the portion of the first metal layer covering the semiconductor columns is removed again;

- the end of the metal layer penetrating to the surface of the laminate are etched back in a metal-specific manner and a third insulating layer is deposited on the laminate with subsequent renewed planar etching;

  or

  the ends of the metal layer penetrating to the surface of the laminate are converted to an insulator by oxidizing or nitriding; and
- finally depositing a second metal layer on the laminate.

Claim 3 (currently amended): The method of claim 2,

~~characterized by the fact that~~

wherein the laminate or individual layers are divided into individual arrays by a lithographic process.

Claim 4 (currently amended): The method of claim 2,

~~characterized by the fact that~~

wherein the growing of the semiconductor columns is carried out electro-chemically.

Claim 5 (currently amended): The method of claim 2,

~~characterized by the fact that~~

wherein the growing of the semiconductor columns is carried out by sputtering.

Claim 6 (currently amended): The method of claim 2,

~~characterized by the fact that~~

wherein the growing of the semiconductor columns is carried out by a CVD process.

Claim 7 (currently amended): The method of claim 2,

~~characterized by the fact that~~

wherein the growing of the semiconductor columns is carried out by vaporization.

Claim 8 (currently amended): The method of claim 2,

~~characterized by the fact that~~

wherein the growing of the semiconductor columns is carried out in ion trace channels of a polymeric film which is subsequently removed.